

## **METHODS FOR MANUFACTURING SEMICONDUCTOR DEVICES AND SEMICONDUCTOR DEVICES HAVING TRENCH ISOLATION REGIONS**

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### **Technical Field**

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The present invention relates to methods for manufacturing semiconductor devices  
and semiconductor devices, and more particularly to methods for manufacturing  
semiconductor devices and semiconductor devices having element isolation regions.

### **Background**

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With further miniaturization of semiconductor devices such as MOS transistors in  
recent years, element isolation regions need to be further miniaturized. To achieve further  
miniaturization of element isolation regions, a trench element isolation technique is  
considered. According to the trench element isolation technique, trenches are provided in a  
substrate between semiconductor elements, and dielectric material is filled in the trenches to  
20 isolate the semiconductor elements from one another.

### **Summary**

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Certain embodiments of the present invention relate to methods for manufacturing  
semiconductor devices and semiconductor devices having element isolation regions in  
which leaks are suppressed.

Embodiments include a method for manufacturing a semiconductor device having a  
trench isolation region, the method including the steps of (a) forming a trench in a  
semiconductor layer; (b) forming a dielectric layer that fills the trench; and

(c) conducting a thermal treatment of the dielectric layer, wherein the thermal treatment is conducted at temperatures of at least 1050°C. In one aspect of certain embodiments, the method may also include a step (d) of forming a well in the semiconductor layer, where the step (c) is conducted before the step (d). In another aspect of certain embodiments, the trench may be formed to include sidewall surfaces and a bottom surface, and the method may further include thermally oxidizing the sidewall surfaces and the bottom surface of the trench.

Embodiments also include a method for manufacturing a semiconductor device having a trench isolation region, the method including forming a trench in a semiconductor layer. A dielectric layer is formed in the trench. The dielectric layer is heated at a temperature of at least 1050°C. In one aspect of certain embodiments, the heating of the dielectric layer may be carried out for a time in the range of 20 to 120 minutes at a temperature in the range of 1050 to 1200°C. In another aspect of certain embodiments, the method also includes forming at least one transistor adjacent to the trench isolation region, the transistor being formed after heating the dielectric layer.

Embodiments also include a method for manufacturing a semiconductor device including a trench isolation region, the method including forming a first layer on a semiconductor substrate and forming a polishing stopper layer above the first layer. At least one trench is formed by etching the first layer while using the polishing stopper layer as a mask. A dielectric layer is formed in and above the trench. The dielectric layer is planarized using the polishing stopper layer as a stopper.

Embodiments also include a semiconductor device including a trench isolation region and transistor element regions, the device including a semiconductor substrate and a first layer formed on the semiconductor substrate. A trench isolation region is formed in the first layer, the trench isolation region including an oxide layer and a dielectric material layer therein. The device also includes transistor element regions separated by the trench isolation region.

Embodiments also include a semiconductor device including a trench isolation region, the device including a semiconductor substrate and an epitaxial growth layer on the

semiconductor substrate. A trench is provided in the epitaxial growth layer, and an annealed dielectric layer is provided in the trench. A trench oxide film is formed between the epitaxial growth layer and the dielectric layer. The device also includes transistor element regions separated by the trench isolation region.

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### Brief Description of the Drawings

Embodiments of the invention are described with reference to the accompanying drawings which, for illustrative purposes, are schematic and not necessarily drawn to scale.

Fig. 1 schematically shows a cross-sectional view of a semiconductor device in accordance with one embodiment of the present invention.

Fig. 2 schematically shows in cross section a step of manufacturing a semiconductor device in accordance with one embodiment of the present invention.

Fig. 3 schematically shows in cross section a step of manufacturing a semiconductor device in accordance with one embodiment of the present invention.

Fig. 4 schematically shows in cross section a step of manufacturing a semiconductor device in accordance with one embodiment of the present invention.

Fig. 5 schematically shows in cross section a step of manufacturing a semiconductor device in accordance with one embodiment of the present invention.

Fig. 6 schematically shows in cross section a step of manufacturing a semiconductor device in accordance with one embodiment of the present invention.

Fig. 7 schematically shows in cross section a step of manufacturing a semiconductor device in accordance with one embodiment of the present invention.

Fig. 8 schematically shows in cross section a step of manufacturing a semiconductor device in accordance with one embodiment of the present invention.

Fig. 9 is a graph showing relations between junction leak currents and trench widths in junctions between n-type impurity diffusion layers and p-type wells.

Fig. 10 is a graph showing relations between junction leak currents and trench widths in junctions between p-type impurity diffusion layers and n-type wells.

**Detailed Description**

A method for manufacturing a semiconductor device having a trench isolation region in accordance with an embodiment of the present invention comprises the following steps

(a) - (c).

- 5           (a) Forming a trench in a semiconductor layer;  
            (b) forming a dielectric layer that fills the trench; and  
            (c) conducting a thermal treatment of the dielectric layer, wherein the thermal treatment is conducted at temperatures of 1050°C or higher.

10           In accordance with the present embodiment, in step (c), the dielectric layer is thermally treated at temperatures of 1050°C or higher. Accordingly, stresses in the dielectric layer can be released. As a result, the generation of cracks in the semiconductor layer can be suppressed, and the generation of leaks is inhibited or suppressed.

            The present embodiment may be particularly useful when, in step (b), the dielectric layer is formed with a film density of 2.1g/cm<sup>3</sup> or greater.

15           The temperature of the thermal treatment (step c) may preferably be 1100°C or higher. Accordingly, the generation of cracks may be inhibited or prevented. As a result, the generation of leaks is inhibited or suppressed.

            The temperature of the thermal treatment (step c) may also preferably be 1250°C or lower.

20           It is preferred that the dielectric layer described above be formed by a high-density plasma CVD method. It is noted that the high-density plasma is plasma with its ion density being  $1 \times 10^{11}/\text{cm}^3$  or greater.

            In certain embodiments, a step (d) of forming a well in the semiconductor layer is included, and in such embodiments step (c) may preferably be conducted before step (d). As  
25           a result, thermal diffusion of the well may be inhibited or prevented.

            Certain embodiments may also include a step (e) of thermally oxidizing the semiconductor layer in the trench, in other words, sidewall surfaces and the bottom surface of the trench, can be thermally oxidized. By the inclusion of step (e), corner sections and edge sections of the semiconductor layer in the trench can be rounded. The temperature at

step (e) may be, for example, at 700 - 1150°C, and more preferably at 950 - 1150°C. In these temperature ranges, corner sections and edge sections of the semiconductor layer can be securely rounded.

5 The semiconductor layer described above may in certain embodiments be an epitaxial growth layer formed on a semiconductor substrate. Such an epitaxial growth layer may preferably have a thickness of 2  $\mu\text{m}$  or greater. As a result, negative influences on the semiconductor elements by diffusion of impurity in the semiconductor substrate can be inhibited or prevented.

10 Embodiments of the present invention are particularly useful when manufacturing a semiconductor device having a trench with a trench width of 0.35  $\mu\text{m}$  or smaller. It is noted that the trench width is a width of the trench at its upper edge section.

It is noted that the "semiconductor layer" may include, for example, a semiconductor substrate and a semiconductor layer (for example, an epitaxial growth layer) formed on a substrate.

15 Certain preferred embodiments of the present invention are described below with reference to the accompanying figures.

A semiconductor device in accordance with an embodiment of present invention is described below. Fig. 1 schematically shows a cross-sectional view of a semiconductor device 100 in accordance with this embodiment.

20 The semiconductor device 100 includes a trench isolation region 30 and MOS transistors 50, 60. A structure of the semiconductor device 100 is as follows.

25 An epitaxial growth layer 12 is formed on a semiconductor substrate 10. A trench isolation region 30 is formed in the epitaxial growth layer 12. The trench isolation region 30 is formed with a dielectric layer 40 filled in a trench 32 that is provided in the epitaxial growth layer 12. A trench oxide film 34 is formed between the epitaxial growth layer 12 and the dielectric layer 40. The trench isolation region 30 defines element regions.

An n-type well 52 is formed in the epitaxial growth layer 12 in one of the element regions. Also, a p-type well 62 is formed in the epitaxial growth layer 12 in the other of the element regions. A p-type MOS transistor 50 is formed in the element region where the n-

type well 52 is formed, and an n-type MOS transistor 60 is formed in the element region where the p-type well 62 is formed.

Next, a method for manufacturing a semiconductor device in accordance with an embodiment of the present invention is described. Figs. 2 through 8 schematically show cross-sectional views of a semiconductor device 100 in manufacturing steps in accordance with the present embodiment.

First, as shown in Fig. 2(a), a layer such as an epitaxial growth layer 12 is formed on a semiconductor substrate 10. The epitaxial growth layer 12 may be formed by flowing, for example, silane ( $\text{SiH}_4$ ) gas, to epitaxially grow silicon on the surface of the semiconductor substrate 10. The epitaxial growth layer 12 may preferably have a thickness of 2  $\mu\text{m}$  or greater, and more preferably 3 - 10  $\mu\text{m}$ .

Next, as shown in Fig. 2(b), a pad layer 14 is formed on the epitaxial growth layer 12. The material of the pad layer 14 may be, for example, silicon oxide, silicon oxide nitride or the like. When the pad layer 14 is formed from silicon oxide, the pad layer 14 can be formed by a thermal oxidation method or a CVD method. When it is formed from silicon oxide nitride, it can be formed by a CVD method or the like. The pad layer 14 has a thickness of, for example, 5 - 20 nm.

Then, a polishing stopper layer 16 is formed over the pad layer 14. The polishing stopper layer 16 may be formed from a single layer structure composed of any one of, for example, a silicon nitride layer, a polycrystal silicon layer and an amorphous silicon layer, or a multiple layered structure composed of at least two types of layers selected from, for example, a silicon nitride layer, a polycrystal silicon layer and an amorphous silicon layer. The polishing stopper layer 16 may be formed by a known method, such as a CVD method. The polishing stopper layer 16 has a sufficient film thickness that can function as a stopper in a chemical-mechanical polishing process performed later, for example, a film thickness of 50 - 200 nm.

Then, as shown in Fig. 3(a), a resist layer R1 having a specified pattern is formed over the polishing stopper layer 16. The resist layer R1 has an opening over a region where a trench 32 is formed.

Then, the polishing stopper layer 16 and the pad layer 14 are etched, using the resist layer R1 as a mask. The etching is conducted by, for example, a dry etching method.

Then, as shown in Fig. 3(b), the resist layer R1 is removed by an ashing procedure. Then, the epitaxial growth layer 12 is etched using the polishing stopper layer 16 as a mask to form a trench 32. The depth of the trench 32 may vary depending upon the design of the device, but may be 300 - 500 nm, for example. The epitaxial growth layer 12 is etched by, for example, a dry etching. A taper angle  $\alpha$  defined by the trench 32 is not particularly limited to any value, but may preferably be 75 - 85 degrees.

Then, as shown in Fig. 4(a), exposed surfaces of the epitaxial growth layer 12 in the trench 32 are oxidized by a thermal oxidation method, to thereby form a trench oxide film 34. The thermal oxidation may function to round and oxide the epitaxial growth layer 12. In other words, the epitaxial growth layer 12 at corner sections 32a (corner sections defined by the trench sidewalls and the trench bottom surface) of the trench 32, and corner sections 32b of protruded sections of the epitaxial growth layer 12 are preferably rounded. In certain embodiments, the temperature of the thermal oxidation is not limited to a particular range as long as the epitaxial growth layer 12 is rounded and oxidized, but may preferably be, for example, 700 - 1150°C, and more preferably 950 - 1150°C. The trench oxide film 34 has a film thickness of, for example, 10 - 100 nm.

Then, as shown in Fig. 4(b), a dielectric layer 40 is formed over the surface of the substrate in a manner to embed the trench 32. The material of the dielectric layer 40 may be, for example, silicon oxide. The film thickness of the dielectric layer 40 may be any thickness that embeds the trench 32 and preferably at least covers the polishing stopper layer 16, for example, the thickness may be 500 - 800 nm. The dielectric layer 40 is preferably deposited by a method that makes the film density to be 2.1 g/cm<sup>3</sup> or greater, and more preferably 2.3 g/cm<sup>3</sup> or greater. Such a method for depositing the dielectric layer 40 includes a high-density plasma CVD method. High-density plasma is plasma with its ion density being  $1 \times 10^{11}$ /cm<sup>3</sup> or greater.

Then, as shown in Fig. 5(a), the dielectric layer 40 is planarized. The planarization is conducted until the polishing stopper layer 16 is exposed. In other words, the dielectric

layer 40 is planarized, using the polishing stopper layer 16 as a stopper. The dielectric layer 40 is planarized by, for example, a chemical-mechanical polishing method.

Next, as shown in Fig. 5(b), the polishing stopper layer 16 is removed, using a heated phosphoric acid, for example. Then, as shown in Fig. 6(a), the pad layer 14 and upper portions of the dielectric layer 40 are isotropically etched.

Next, as shown in Fig. 6(b), a sacrificial oxide layer 20 is formed on exposed surfaces of the epitaxial growth layer 12 by a thermal oxidation method. The sacrificial oxide layer 20 may have a film thickness of 10 - 20 nm, for example.

Then, the dielectric layer 40 is subject to a thermal treatment. By thermally treating the dielectric layer 40, stresses in the dielectric layer 40 are released. As a result, the generation of cracks in the epitaxial growth layer, which may be caused by stresses of the dielectric layer 40, can be suppressed, and leaks can be suppressed. The thermal treatment is conducted at temperatures of 1050°C or higher, and more preferably 1100°C or higher. The generation of leaks can be securely prevented when the thermal treatment is conducted at temperatures of 1100°C or higher. Also, the thermal treatment may preferably be conducted at temperatures of 1250°C or lower in view of the heat resistance of the thermal treatment apparatus. The thermal treatment may be conducted in an inactive gas atmosphere, or an oxygen atmosphere. Preferably the thermal treatment may be conducted in an inactive gas atmosphere that includes oxygen gas in the range of 0.1 volume % to 10 volume %. The thermal treatment is preferably conducted for, for example, 20 - 120 minutes, and more preferably 40 - 80 minutes. In this manner, the trench isolation region 30 is formed. And after the thermal treatment, the film density of the dielectric layer is at least 2.1g/cm<sup>3</sup>, and more preferably 2.3g/cm<sup>3</sup> or greater.

Next, as shown in Fig. 7(a), a resist layer R2 having a specified pattern is formed. The resist layer R2 defines an opening in a region that becomes an n-type well. An n-type impurity such as phosphorous and arsenic is implanted in the epitaxial growth layer 12 one or more times, using the resist layer R2 as a mask, to thereby form an n-type well 52 in the epitaxial growth layer 12. Subsequently, the resist layer R2 is removed.



Next, as shown in Fig. 7(b), a resist layer R3 having a specified pattern is formed. The resist layer R3 defines an opening in a region that becomes a p-type well. A p-type impurity such as boron is implanted in the epitaxial growth layer 12 once or plural times, using the resist layer R3 as a mask, to thereby form a p-type well 62 in the epitaxial growth layer 12. Subsequently, the resist layer R3 is removed.

Then, as shown in Fig. 8, the sacrificial oxide film 20 and upper portions of the dielectric layer 40 are isotropically etched. Next, as shown in Fig. 1, a p-type MOS transistor 50 and an n-type MOS transistor 60 are formed in the respective element regions by a known method.

Certain embodiments may include one or more of the effects described below.

Certain embodiments of the present invention include a step of thermally treating the dielectric layer 40 at temperatures of 1050°C or higher. Accordingly, stresses in the dielectric layer 40 with a high film density can be relieved. As a result, the generation of cracks in the epitaxial growth layer 12, which may be resulted from the dielectric layer 40, can be suppressed. Therefore, the generation of leaks is suppressed. Also, when the temperature of the thermal treatment is 1100°C or higher, the generation of leaks can be inhibited or securely prevented.

It is noted that, if the dielectric layer is not thermally treated at all or treated at temperatures other than the temperatures described above, there is a tendency that cracks are generated in the epitaxial growth layer in the narrow trench due to stresses in the dielectric layer, and leaks are generated.

In certain embodiments, the thermal treatment step for the dielectric layer 40 is conducted before wells are formed. As a result, wells will not diffuse due to the thermal treatment of the dielectric layer 40.

The method embodiment described above is particularly useful in manufacturing a semiconductor device having a trench with a trench width being 0.35  $\mu\text{m}$  or less, and more preferably 0.3  $\mu\text{m}$  or less.

In certain embodiments, when the epitaxial growth layer 12 has a thickness of 2  $\mu\text{m}$  or greater, the generation of negative influences on the semiconductor elements can be

inhibited or securely prevented even when the impurity in the semiconductor substrate 10 diffuses into the epitaxial growth layer 12.

Differences in the generation of junction leaks have been examined for cases in which a dielectric layer that fills a trench is subject to a thermal treatment and for cases in 5 which a thermal treatment is not conducted.

Fig. 9 is a graph showing relations between junction leak currents and trench widths in junctions between n-type impurity diffusion layers and p-type wells. It is noted that N+ (P well) leaks are observed for the junction leak currents. In other words, electron leaks are observed. Also, a voltage applied to the semiconductor substrate with respect to the n- 10 type impurity diffusion layer is 2.7 V.

Fig. 10 is a graph showing relations between junction leak currents and trench widths in junctions between p-type impurity diffusion layers and n-type wells. It is noted that P+ (N well) leaks are observed for the junction leak currents. In other words, hole leaks are observed. Also, a voltage applied to the semiconductor substrate with respect to the p-type 15 impurity diffusion layer is -2.7 V.

It is noted that • marks indicate data obtained when the thermal treatment temperature is at 1100°C. □ marks indicate data obtained when the thermal treatment temperature is at 1000°C. × marks indicate data when the thermal treatment of the dielectric layer is not conducted. The trench width is a width at an upper section of the trench.

Test samples were manufactured according to the method embodiment described 20 above. Processing conditions include the following. The dielectric layer was formed by a high-density plasma CVD method. The dielectric layer was thermally treated for 30 minutes in a nitrogen atmosphere under atmospheric pressure.

It is observed from Fig. 9 and Fig. 10 that, when the dielectric layer is not thermally 25 treated, junction leak currents amount to levels on the order of  $1\text{E} - 10$  A, and junction leaks are generated when the trench widths become narrow ( $0.35\text{ }\mu\text{m}$  in Fig. 9, and  $0.3\text{ }\mu\text{m}$  in Fig. 10). It is noted that the noise levels are on the order of  $1\text{E} - 11$  A. In contrast, when the dielectric layer is thermally treated at 1100°C, junction leak currents remain at levels on the order of  $1\text{E} - 11$  A (at noise levels), even when the trench width is narrow. In view of the

above, it is understood that, when the dielectric layer is thermally treated at 1100°C or higher, junction leaks are securely prevented.

It is also observed from Fig. 9 and Fig. 10 that, an increase in the junction leak current cannot be suppressed even when the dielectric layer is thermally treated if the thermal treatment temperature is at 1000°C.

The present invention is not limited to the embodiments described above, and many modifications can be made without departing from the subject matter of the present invention.

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